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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/058,959	01/29/2002	William Edward Floro	01AB089	4640

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EXAMINER	
RIOS CUEVAS, ROBERTO JOSE	
ART UNIT	**PAPER NUMBER**
2836	

DATE MAILED: 04/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/058,959	FLORO ET AL.	
	Examiner	Art Unit	
	Roberto J Rios	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 6-21* is/are rejected.

7)☒ Claim(s) *4 and 5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 May 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 2, 12, 13 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Caulkins (US patent 6,473,355).

As per claims 1 and 12, Caulkins teaches a method of operating and a memory system having power backup comprising: a backup supply line (inside UPS 301) receiving a backup voltage when a line voltage is lost; volatile memory (303) receiving voltage from the backup supply line, the memory providing a low power operating mode controlled by volatile data held in the memory; and a voltage supervisory circuit (305) communicating with the backup supply line and the volatile memory, wherein once the voltage of the backup supply (301A) drops below a predetermined level, volatile memory device is orderly shut down (col. 10, line 22; Figure 3A). The term "orderly shut down" is interpreted to mean termination of power after specific tasks are accomplished in a predetermined order. Moreover, termination or interruption of power is well known in the art to be done through a switch means. Caulkins teaches the voltage supervisory circuit comprising an electronic control logic chip that shut downs the volatile memory

device in an orderly manner. Thus, an electronic controlled switching means is inherently used to selectively disconnect the supply of backup power from the memory; otherwise an orderly shutdown could never be accomplished.

As per claims 2 and 13, Caulkins teaches a backup voltage source connected to the backup supply line consisting of a battery (Figure 3A).

As per claim 20, Caulkins teaches a memory system capable of receiving primary power from a primary power source and backup power from a backup power source, the memory system comprising: a volatile memory (303) that stores data; at least one power line coupled to the volatile memory and capable of communicating the primary and backup power to the volatile memory (Figure 3A); a circuit (305) coupled to at least one of the volatile memory and the at least one power line, wherein the circuit determines when both the primary and backup power have been disrupted and (primary loss and battery below optimum operating voltage), upon making such a determination, volatile memory device is orderly shut down and operates to prevent the volatile memory from receiving the backup power until after a time at which the primary power has recovered (col. 10, lines 22). The term "orderly shut down" is interpreted to mean termination of power after specific tasks are accomplished in a predetermined order. Moreover, termination or interruption of power is well known in the art to be done through a switch means. Caulkins teaches the voltage supervisory circuit comprising an electronic control logic chip that shut downs the volatile memory device in an orderly manner. Thus, an electronic controlled switching means is inherently used to selectively

disconnect the supply of backup power from the memory; otherwise an orderly shutdown could never be accomplished.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3, 6, 9-11,14-16 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Caulkins in view of Lee et al (US patent 4,730,121).

As per claims 3 and 14, Caulkins teaches disconnecting the battery from the memory but does not specifically teaches the claimed latching means. However, Lee et al (herein after Lee) teach a memory system including a latching means connected between a voltage supervisory circuit and an electronically controlled switch whereby the electronically controlled switch is latched to disconnect a backup supply line from the volatile memory even after restoration of backup voltage to the normal backup voltage while the memory system is not receiving line voltage (Figure 1; col. 11, line 40).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the memory system of Caulkins with the latching arrangement of Lee for the purpose isolating the battery from the memory and provide immunity form voltage spikes in the line voltage.

As per claim 15, Lee teaches unlatching the signal controlling the electronically controlled switch, thereby allowing reconnection of the backup battery to the volatile memory, after restoration of line voltage (col. 11, line 40).

As per claims 6 and 16, Lee teaches the voltage supervisory circuit receiving backup voltage (VL) from the backup supply line via the electronically controlled switch (Figure 1).

As per claims 9 and 19, Caulkins teaches the memory system but does not specifically disclose the claimed low power arrangement arrangement. However, Lee teaches a microprocessor communicating with the volatile memory; a low power warning circuit indicating a reduction of line power; and wherein the microprocessor executes a control program to read a low power warning signal from the low power warning circuit and in response to that signal to write to the volatile memory the volatile data to put the volatile memory into the low power operating mode (col. 8, line 21).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the memory system of Caulkins with the low power arrangement of Lee for the purpose of putting the volatile memory into a low power battery backed operating mode.

As per claim 10, Caulkins teaches the backup voltage being from a battery but does not specifically disclose using a voltage converter between the battery and the volatile memory. However, the Examiner takes official notice that it is well known in the art to place a voltage converter between a backup battery and a volatile memory. The Examiner wants to point out that applicant has failed to seasonably traverse this official

notice taken in the last office action mailed on 10/06/2003. If applicant does not seasonably traverse the well-known statement during examination, then the object of the well-known statement is taken to be admitted prior art. *In re Chevenard*, 139 F.2d 71, 60 USPQ 239 (CCPA 1943). A seasonable challenge constitutes a demand for evidence made as soon as practicable during prosecution. Thus, applicant was charged with rebutting the well-known statement in the reply after the Office action in which the well-known statement was made (I.e., Arguments filed on 12/29/2003), MPEP§ 2144.03

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the teachings of Caulkins such that a voltage converter is placed between a backup battery and a volatile memory for the purpose of providing proper operating voltage to said memory.

As per claim 11, Caulkins teaches the volatile memory being DRAM (col. 17, line 53).

5. Claims 7, 8, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Caulkins in view of Zandveld et al (US patent 4,841,474).

As per claims 7, 8, 17 and 18, Caulkins teaches the memory system but does not specifically disclose the claimed latching arrangement. However, Zandveld et al (herein after Zandveld) teach a microprocessor; latching means connected between a voltage supervisory circuit and the microprocessor to provide a signal to the microprocessor indicating that the backup supply line has previously been disconnected from the volatile memory even after the backup supply line has been reconnected to the volatile

memory while the memory system is not receiving line voltage; whereby a control program executed on the microprocessor can determine after a power up the integrity of data in the volatile memory and said latch is reset after restoration or power (Figure 4; col. 9, line 53+; claim 1).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the memory system of Caulkins with the latching arrangement of Zandveld for the purpose of determining data integrity.

6. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Caulkins in view of Culbert (U.S. patent 5,557,777).

As per claim 21, Caulkins teaches the volatile memory device being orderly shut down and controlling whether the volatile memory receives backup power (col. 10, lines 22). The term "orderly shut down" is interpreted to mean termination of power after specific tasks are accomplished in a predetermined order. Moreover, termination or interruption of power is well known in the art to be done through a switch means. Caulkins teaches the voltage supervisory circuit comprising an electronic control logic chip that shut downs the volatile memory device in an orderly manner. Thus, an electronic controlled switching means is inherently used to selectively disconnect the supply of backup power from the memory; otherwise an orderly shutdown could never be accomplished. Caulkins does not specifically teaches the voltage supervisory circuit being capable of providing a signal indicating that the data is no longer reliable. However, Culbert teaches a volatile memory arrangement comprising a voltage supervisory circuit that determines if an orderly shutdown (i.e., termination of power)

occurs, wherein the voltage supervisory circuit being capable of providing a signal indicating that the data is no longer reliable (col. 2, line 63- col. 3, line 37).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the memory system of Caulkins with the voltage supervisory circuit of Culbert for the purpose of performing a start-up based on the validity of said data.

Allowable Subject Matter

7. Claims 4 and 5 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The reasons for the indication of allowable subject matter were previously explained in the last office non-final first action.

Response to Arguments

9. Applicant's arguments filed 12/29/2003 have been fully considered but they are not persuasive.

Applicant argues that the examiner failed to provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art. Applicant also argues that they were unable to find any disclosure within Caulkins that any switch is used to interrupt or disconnect a backup power supply line. The Examiner respectfully disagrees. Caulkins teaches that once the voltage of the backup supply (301A) drops below a predetermined level, volatile memory device is orderly shut down (col. 10, line

22; Figure 3A). The term "orderly shut down" is interpreted to mean termination of power after specific tasks are accomplished in a predetermined order. Moreover, termination or interruption of power is well known in the art to be done through a switch means. Caulkins teaches the voltage supervisory circuit comprising an electronic control logic chip that shut downs the volatile memory device in an orderly manner. Thus, an electronic controlled switching means is inherently used to selectively disconnect the supply of backup power from the memory; otherwise an orderly shutdown could never be accomplished. Applicant's attention is directed to previously cited U.S. patent 5,241,508 for a background explanation of a volatile memory power backup means where an electronically controlled switch is selectively controlled by a power controller.

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Communication with PTO

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Roberto Rios whose telephone number is (571) 272-2056. In the event that Examiner Rios cannot be reached, his supervisor, Brian Sircus may be contacted at (571) 272-2800, ext. 36. The fax number for Before-Final communications and After-Final communications is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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